Amendment to the Claims:

Please cancel claims 25-43 and 45-56, without prejudice. Please add claims 57-65 as recited below.

57. (Currently Added) A process for forming device isolation for a semiconductor assembly comprising:

forming a first trench having sidewalls into a semiconductor substrate;

forming a single oxidizable layer lining a surface of the first trench;

forming spacers of oxidizable material along the sidewalls of the first trench over and in direct contact with the single oxidizable layer;

forming a second trench into the semiconductor substrate at the bottom of the first trench using the spacers as an etching guide, wherein an overall depth of the first and second trenches is two times a depth of a bordering diffusion region determined by an area containing at least approximately 90% concentration of conductive atoms;

forming an insulative material in the first and second trenches at least partially by substantially consuming the oxidizable material of the spacer and the single oxidizable layer.

58. (Currently Added) The process as recited in claim 57, wherein forming the insulative material comprises annealing the semiconductor assembly in the presence of an oxidizing agent.

59. (Currently Added) The process as recited in claim 57, wherein said process uses only one mask to form the device isolation.

60. (Currently Added) A process for forming device isolation for a semiconductor assembly comprising:

forming a first trench having sidewalls into a semiconductor substrate;

forming a single semiconductive layer lining a surface of the first trench;

forming spacers of semiconductive material along the sidewalls of the first trench over and in direct contact with the single oxide layer;

forming a second trench into the semiconductor substrate at the bottom of the first trench using the spacers as an etching guide, wherein an overall depth of the first and second trenches is two times a depth of a bordering diffusion region determined by an area containing at least approximately 90% concentration of conductive atoms;

forming an insulative material in the first and second trenches at least partially by substantially consuming the semiconductive material of the spacer and the single semiconductive layer.

61. (Currently Added) The process as recited in claim 60, wherein forming the insulative material comprises annealing the semiconductor assembly in the presence of an oxidizing agent.

62. (Currently Added) The process as recited in claim 60, wherein the process uses only one mask to form the device isolation.

63. (Currently Added) A process for forming device isolation for a semiconductor assembly comprising:

forming a first trench having sidewalls into a semiconductor substrate;

forming a single oxide layer lining a surface of the first trench;

forming spacers of silicon material along the sidewalls of the first trench over and in direct contact with the single oxide layer;

forming a second trench into the semiconductor substrate at the bottom of the first trench using the spacers as an etching guide, wherein an overall depth of the first and second trenches is two times a depth of a bordering diffusion region determined by an area containing at least approximately 90% concentration of conductive atoms;

forming an oxide filler in the first and second trenches at least partially by substantially consuming the silicon material of the spacer and the single oxide layer; and

planarizing the oxide filler.

64. (Currently Added) The process as recited in claim 63, wherein forming the oxide filler comprises annealing the semiconductor assembly in the presence of an oxidizing agent.

65. (Currently Added) The process as recited in claim 63, wherein the process uses only one mask to form the device isolation.